

ABSTRACT OF THE DISCLOSURE

A memory device such as a $6F^2$ memory device includes isolation trenches that are
5 formed generally parallel to and along associated strips of active area. A conductive bit line is
recessed within each isolation trench such that the uppermost surface of the bit line is recessed
below the uppermost surface of the base substrate. A bit line contact strap electrically couples
the bit line to the active area both along a vertical dimension of the bit line strap and along a
horizontal dimension across the uppermost surface of the base substrate.

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